Please amend the Application as set forth in the Amendments below.

In the Drawings:

Please substitute the following replacement drawing for Figure 8, submitted herewith as Attachment B. No new matter is added.

REMARKS

Receipt is acknowledged of the Office Action mailed April 27, 2006. Applicant respectfully requests reconsideration of the present application in view of the foregoing amendment, and the remarks which follow. No new matter is added with the amendments, which are fully supported by the specification.

Claims 1-2, 5-6, and 8-11 have been amended. Claims 1-11 are pending in the application.

Applicant thanks the Examiner for acknowledging the claim for foreign priority and the Information Disclosure Statement mailed on 06/28/2005. In addition, Applicant thanks the Examiner for the indication that claims 2-5 and 10 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Objections to the Drawings:

The examiner objected to Figures 5 and 8. Specifically, the examiner argued that the drawings were inconsistent with lines 1-3 on page 13 of the specification. In response, that section of the specification has been amended. Regarding the examiner's comment regarding the SACLK pulse signal, the pulse signal is output through the first delay block 51, the NAND gate ND13, and the inverter INV12.

Regarding the issue about the leading and trailing edges of GIOSTP, applicant submits the following explanation of Figs. 5 and 8. Initially, both TMCOMP and GIOSTP are low. Therefore, the output of ND12 is high. The output of the first delay block [51] is low because the delay block comprises an odd number of inverters [Page 12, lines 20-21]. Consequently, the output of ND13 is high and SACLK is low.

Next, TMCOMP become high while GIOSTP remains low. The output of ND12 is still high and all other logic values are unchanged. However, ND12 becomes low once both TMCOMP and GIOSTP are high. The first delay block [51] now produces a high signal. ND12 becomes high when the trailing edge of GIOSTP, sending GIOSTP low.

During the period when the first delay block [51] is still producing high output, the output of ND13 will be low, producing a high pulse for SACLK. The SACLK pulse will remain high as long as the output of the delay block [51] is high. As depicted in the amended version of Fig. 8, the trailing edge of GIOSTP is aligned with the SACLK pulse.

Objections to the Abstract:

The examiner objected to the abstract for containing certain informalities. In response, a replacement Abstract has been filed, appended to this paper as Attachment A.

Objections to the Specification:

The examiner objected to the specification for containing certain informalities. In response, several paragraphs in the specification have been replaced.

Objections to the Claims:

The examiner objected to claims 1 and 6 for containing certain informalities. In response, claims 1 and 6 have been amended.

Claim Rejections under 35 U.S.C. § 112, ¶1 – Best Mode:

The examiner rejected claims 1, 8, and 9 under 35 U.S.C. § 112, ¶1 as failing to comply with the best mode requirement. This rejection is respectfully traversed. As set forth in MPEP 706.03(c), an examiner cannot make a "best mode" rejection without providing a basis for holding that the best mode has been concealed, e.g., the quality of applicant's disclosure is so poor as to effectively result in concealment. Here, the

examiner has provide no evidence of concealment. Second, a "best mode" rejection should only be made if a feature considered critical or essential by applicant to the practice of the claimed invention is missing from the claim. Here, the examiner has not alleged that any features are missing, but merely points to an alleged inconsistency in the specification.

Moreover, as stated in MPEP 2165.03, it is extremely rare that a best mode rejection properly would be made in *ex parte* prosecution. The examiner should assume that the best mode is disclosed in the application, unless evidence is presented that is inconsistent with that assumption. In order to properly establish a best mode rejection, an examiner must determine whether the inventor knew that one mode was better than another, and if so, whether the disclosure is adequate to enable one of ordinary skill in the art to practice the best mode. A best mode rejection is proper only when the first inquiry can be answered in the affirmative and the second inquiry answered in the negative with reasons to support the conclusion that the specification is nonenabling with respect to the best mode. Here, the examiner did not perform the required analysis and presented no reasons to support a best mode rejection.

In view of the above explanation, Applicant requests the examiner to reconsider and withdraw the § 112, ¶1, best mode rejection.

Claim Rejections under 35 U.S.C. § 112, ¶1 – Enablement:

The examiner rejected claims 1, 8, and 9 under 35 U.S.C. § 112, ¶1 as based on a disclosure that is not enabling. This rejection is respectfully traversed for the following reasons.

As set forth in M.P.E.P. 2164.01, the test of enablement is whether one reasonably skilled in the art could make or use the invention from the disclosure in the patent coupled with information known in the art without undue experimentation. Here, the examiner

has never explained why one reasonably skilled in the art would be unable to make or use the invention.

Unlike the conventional I/O compression test circuit, the present invention discloses the use of two strobe signals [SACLK/SACLKD] to respectively control timing of the test blocks [Fig. 3: 10/20/30/40] and the driving block [70]. By providing improved synchronization, the present invention compensates for skew. It also compensates for "glitch" errors, because glitches are possible when skew creates timing gaps between signals. To more clearly describe the present invention, the expression "sampling clock signals," this term has been amended to – strobe signals – throughout the entire specification.

In view of the above explanation, Applicant requests the examiner to reconsider and withdraw the § 112, ¶1, enablement rejection.

Claim Rejections under 35 U.S.C. § 112, ¶1 – Scope of Enablement:

The examiner rejected claims 1, 8, and 9 under 35 U.S.C. § 112, ¶1, because the scope of the claims is not commensurate with the scope of the enabling disclosure. This rejection is respectfully traversed for the following reasons.

As set forth in M.P.E.P. 2164.08, the determination of the propriety of a rejection based upon the scope of a claim relative to the scope of the enablement involves two stages of inquiry. The first is to determine how broad the claim is with respect to the disclosure. The entire claim must be considered. The second inquiry is to determine if one skilled in the art is enabled to make and use the entire scope of the claimed invention without undue experimentation.

Here, the examiner has not explained why claims 1, 8, and 9 are rejected, instead presenting objections to sections of the specification. The examiner never attempts to define the breadth of the claims, merely alleging that the specification enables the strobe

block [Fig. 1: 6] but does not enable the first delay block [Fig. 5: 51]. While the examiner alleges that a critical feature is "in question," the examiner neither poses an actual question nor indicates why "any person skilled in art" would be unable to make or use a delay block.

In view of the above explanation, Applicant requests the examiner to reconsider and withdraw the § 112, ¶1, scope of enablement rejection.

Claim Rejections under 35 U.S.C. § 112, ¶2

The examiner rejected claim 8 under 35 U.S.C. § 112, ¶2 for being indefinite. In response, claim 8 has been amended to more clearly describe generation of strobe signals by the control block. The "test timing" phrase objected to by the examiner has been deleted from claim 8. It is submitted that claim 8 complies with § 112, ¶2.

Claim Rejections under 35 U.S.C. § 102(a)

The examiner rejected claims 1, 6-9, and 11 under 35 U.S.C. § 102(a) as anticipated the admitted prior art, hereafter APA. Applicant respectfully traverses this rejection for at least the following reasons.

The known I/O compression test circuit [Page 2, line 8] comprises a strobe block [Fig. 1: 6] sending an output signal to a detection block [5] synchronously with respect to a strobe signal STN [Page 2, lines 15-16]. In contrast, the present invention provides a strobe signal SACLK [Page 12, lines 13-15] and a delay strobe signal SACLKD [Page 12, line 16]. The strobe signal SACLK controls the timing of the test blocks 10, 20, 30, and 40, [Page 13, lines 6-7] while the delay strobe signal SACLKD controls timing for the driving block 70 [Page 13, lines 8-11]. Signals SACLK and SACLKD are now respectively recited in independent claim 1 as the first strobe signal and the second strobe signal. Applicant respectfully submits that the APA, having only a single strobe signal, fails to teach or suggest this recited limitation.

In addition, APA clearly lacks a reset signal. As depicted in Fig. 3, the present invention generates a reset signal in a control block [50] and then applies that signal to a decision block [60]. The control block serves as a corrector for initialization, reducing the impact of skew [Page 12, lines 22-24] and the reset signal RESET initializes an output terminal of the decision block 60 [Page 13, lines 12-13]. None of these limitations are taught or suggested by APA.

Accordingly, Applicant respectfully requests the Examiner to withdraw the rejection of claims 1, 6-9, and 11 under 35 U.S.C. §102(a) as anticipated by APA. Further, since claim 1 is now in allowable form, Applicant requests withdrawal of the objections to claims 2-5 and 10.

CONCLUSION

In view of the above amendment and remarks, applicant respectfully requests that all objections and rejections be withdrawn and that a notice of allowance be forthcoming. The Examiner is invited to contact the undersigned attorney for applicant at 202-912-2503 for any reason related to the advancement of this case.

Respectfully submitted,

Date: July 27, 2006

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MARKED-UP VERSION SHOWING CHANGES

Abstract of the Disclosure

The I/O compression test circuit performs ~~the test~~ tests on [[the]] global I/O lines divided into groups [[when]] after failure occurs, thereby improving [[the]] repair efficiency. ~~Also, since the~~ The configuration of the test circuit is simplified by using a reset circuit, reducing the delay time ~~generated by a logic circuit device is reduced~~, and thereby decreasing test time. Additionally, two ~~sampling clock~~ strobe signals enable ~~memory cells~~ the I/O compression test circuit to perform a stable operation ~~on skew between global I/O lines or a glitch generated in internal circuits~~.